REMARKS

The claims are claims 1, 4, 5, 11 and 13.

Claims 1 and 13 are amended. Claim 10 is newly canceled. Claims 1 and 13 are amended to change "arithmetic circuit" to "adder/subtractor circuit." This new term corresponds to adder/subtractor 420 illustrated in Figure 4, adder/subtractor 520 illustrated in Figure 5 and adder/subtractor 620 illustrated in Figure 6. The Applicants respectfully submit that this term has a limited meaning established in the art.

Claims 1, 4, 5, 11 and 13 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Saishi et al U.S. Patent No. 6,167,419 and Pitsianis et al U.S. Patent Application Publication No. 2003/00088601. The FINAL REJECTION states that Saishi et al discloses rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving first product, and a carry input to a mid-position receiving rounding value to form the intermediate result at elements 803, 806, and 807 in Figure 8 and column 8, lines 11 to 63.

Claims 1 and 13 recite subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 1 recites "combining the first product with the second product to form a combined product and rounding the combined product to form an intermediate result via an adder/subtractor circuit." Claim 13 similarly recites "an adder/subtractor circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." The innovation of the application is combining operations normally requiring two hardware circuits into a single hardware circuit.

The two combined operations are the sum/difference of the two products and rounding the result. The Applicants respectfully submit that the recited adder/subtractor circuit corresponds to: adder/subtractors 420, 520 and 620 disclosed in this application; addition means 109, addition means 209, first subproduct addition means 306/second subproduct addition means 308, first subproduct addition means 406/second subproduct addition means 408, first subproduct addition means 506/second subproduct addition means 508 disclosed in Saishi et al; and subtractor 623, adder 625, adder 723, subtractor 725, adder block 1723, adder block 1725, adder block 1823 and adder block 1825 of Pitsianis et al. Neither Saishi et al nor Pitsianis et al teach combining two products and rounding in a single adder/subtractor circuit as recited in claims 1 and 13. Firstly, Saishi et al teaches only one product. Saishi et al teaches rounding the multiplication result 104 in addition means 109 and rounding the multiplication result 204 in addition means 209. Figures 3 to 5 of Saishi et al illustrate combining the partial product sums of a single product computation with rounding in first subproduct addition means 306/406/506. Thus Saishi et al fails to teach the claimed combination of two products and rounding recited in claims 1 and 13. Pitsianis et al teaches production of two products but does not teach a single adder/subtractor circuit combining two products and rounding. Figure 6 of Pitsianis et al teaches combining products in subtractor 623 and adder 625, and rounding the selection and rounder circuit 627. Figure 7 of Pitsianis et al teaches combining products in adder 723 and subtractor 725, and rounding in selection and rounder circuit 727. Figure 17 of Pitsianis et al teaches combining products in adder block 1723 and adder block 1725, and rounding in selection and rounder circuit 1727. Figure 18 of Pitsianis et al teaches combining products in adder block 1823 and adder block 1825, and rounding

in selection and rounder circuit 1827. The Applicants respectfully submit that both Saishi et al and Pitsianis et al teach the adder/subtractor circuit recited in claims 1 and 13 without teaching the particularly recited combination of two products and rounding. Accordingly, claims 1 and 13 are not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 1 and 13 recite further subject matter not made obvious by the combination of Saishi et al and Pitsianis et al. Claim 1 recites "a carry input to a mid-position receiving said rounding value to form the intermediate result." Claim 13 similarly recites "a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction." Saishi et al fail to teach this use of a mid-position carry input for the recited rounding. Saishi et al states at column 8, lines 27 to 35 (within the portion cited in the FINAL REJECTION):

> "When the range indicated by the bit range 804 of the multiplication result 803 is desired to be cut out, and when it is assumed that the predetermined rounding position 811 is basically located at the mth bit from the least significant bit in consideration of the fact that a shift count required for a shift operation for cutting out is indicated by a right shift 809 of kbits, a signal having '1' at the (m+k)th bit is generated as the rounding signal. In other words, the rounding position is shifted to the left by k bits."

This clearly teaches that the rounding position is selected by the rounding generator generating a rounding signal shifted to correspond to the later shift of the rounded product. One skilled in the art would understand the recited "shifted to the left by k bits" to be a multibit signal having 0's shifted into the k least significant bits to place a single 1 bit in the desired rounding position. Figures 1 to 5 of Saishi et al show this rounding signal applied to a normal data input of an

addition means. Saishi et al never states that the rounding signal is input to "a carry input to a mid-position" as recited in claim 1 or to "a mid-position carry input" as recited in claim 13. The FINAL REJECTION fails to cite any portion of Saishi et al as making obvious the recited mid-position carry input. One skilled in the art would understand Saishi et al to teach supply of the rounding signal to an ordinary multi-bit data input of the adder. The left shifted 1 generated by the rounding signal generator is thus supplied to a data input and not to the carry input recited in claims 1 and 13. Thus Saishi et al teaches achieving the same result of this invention using a different method step or different apparatus. While the FINAL REJECTION states that this is disclosed in Saishi et al, in fact neither addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406, nor first subproduct addition means 506 illustrate the "carry input to a mid-position" recited in claim 1 and or the "mid-position carry input" recited in claim 13. The description of these parts in Saishi et al indicated that the rounding signal is supplied to a data input of the corresponding addition means. Saishi et al states at column 6, lines 11 to 14:

> "The multiplication result 104 and the rounding signal 106 are input to the addition means 109, and the addition means 109 outputs the multiplication result 110 obtained after rounding."

Saishi et al states at column 10, lines 50 to 53:

> "The subproducts 305 and the rounding signal 315 are added by the first subproduct addition means 306."

This disclosure with the teaching of Saishi et al that the rounding signal is "shifted to the left by k bits" makes clear

that the rounding signal is supplied to a multibit input of addition means 109, addition means 209, first subproduct addition means 306, first subproduct addition means 406 and first subproduct addition means 506 rather than the "carry input to a mid-position' recited in claim 1 or the "mid-position carry input" recited in claim 13. The FINAL REJECTION does not allege that Pitsianis et al makes obvious this subject matter. Accordingly, claims 1 and 13 are not made obvious by the combination of Saishi et al and Pitsianis et al.

Claims 4, 5 and 11 are allowable by dependence upon respective allowable base claims 1 and 13.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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